					Course Code: B20EC3101
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R 20**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		INTERNET OF THINGS			
		Electronics and Communication Engineering			
Time: 3 Hrs.				**Max. Marks:70**	
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Explain the typical Embedded system architecture with relevantdiagram?	**1**	**2**	**7**
	b).	Illustrate an application-specific Embedded system with suitableexamples?	**1**	**2**	**7**
		OR			
2.	**a).**	Explain the characteristics of embedded systems	**1**	**2**	**7**
	b).	Discuss about Real time clock with respect to an Embedded Hardware?	**1**	**2**	**7**
		UNIT-II			
3.	**a).**	Explain about serial communication devices and parallel device ports?.	**1**	**2**	**7**
	b).	Discuss the significance of Watchdog timer in an Embedded System.	**1**	**2**	**7**
		OR			
4.	**a).**	What is a Device Driver? Explain different types of device drivers anduse of them	**2**	**2**	**7**
	b).	Explain about memory organization in Embedded system	**2**	**2**	**7**
		UNIT-III			
5.	**a).**	Draw and explain about Physical Design & Logical Design of IoT	**1**	**2**	**7**
	b).	Define IoT and mention different Characteristics of IoT	**1**	**2**	**7**
		OR			
6.	**a).**	Explain in details about IoT protocols	**1**	**2**	**7**
	b).	Differences and Similarities between M2M and IoT.	**1**	**2**	**7**
		UNIT-IV			
7.	**a).**	Name and explain in detail about any two communication concepts	**3**	**2**	**7**

	b).	Explain about the following a) Ultrasonic Sensor b) IR Sensor c) Temperature & Humidity	**3**	**2**	**7**
		OR			
8.		Explain the Basic building blocks of an IoT Device & relate it withexemplary device.	**3**	**3**	**14**
		UNIT-V			
9.	**a).**	Explain in detail about Web Application Messaging Protocol(WAMP).	**4**	**3**	**7**
	b).	Demonstrate the role of Cloud based communication & Data AnalyticsIn IoT	**4**	**3**	**7**
		OR			
10.		Analyze IoT Design Methodology with a use case.	**4**	**4**	**14**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

			Course Code: B20EC3102		
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)		**R 20**	
		III B.Tech. I Semester MODEL QUESTION PAPER			
		ANTENNAS & WAVE PROPAGATION			
		Electronics and Communication Engineering			
		Time: 3 Hrs.		**Max. Marks:70**	
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Derive expressions for the EM fields radiated by an λ/2 Dipole.	**1**	**3**	**7**
	b).	Compute the directivity of a λ/4 Monopole.	**1**	**3**	**7**
		OR			
2.	**a).**	Compute the radiation resistance of a half wave dipole.	**1**	**3**	**7**
	b).	Explain about different types of current distribution on linear antennas.	**1**	**2**	**7**
		UNIT-II			
3.	**a).**	What are Broadside and End-fire arrays? Obtain expressions for BWFN and HPBW in both cases.	**2**	**3**	**7**
	b).	A Broadside array has a BWFN of 40deg. Compute the BWFN in degrees if the same array is excited in End-fire fashion.	**2**	**4**	**7**
		OR			
4.	**a).**	Show that in a uniform linear array, the first side lobe is down the principal Maximum by 13.5dB.	**2**	**4**	**7**
	b).	Explain the technique of pattern multiplication with examples.	**2**	**2**	**7**
		UNIT-III			
5.	**a).**	With a neat diagram, explain the operating principles of Rhombic antenna. List out the disadvantages of a Rhombic antenna.	**3**	**2**	**7**
	b).	Compute the optimum values of length, height and tilt angle of a Rhombic antenna if the angle of elevation alpha at which the EMenergy leaves the antenna is 30deg.	**3**	**4**	**7**
		OR			
6.	**a).**	Explain in detail about the various feed mechanisms of antennas with Parabolic reflectors.	**3**	**2**	**7**
	b).	Derive an expression for the expression of the impedance of the Slot antenna.	**3**	**3**	**7**
		UNIT-IV			

7.	**a).**	Explain in detail about the slotted line method of antenna input impedance measurement.	**4**	**2**	**7**
	b).	Explain the method of measuring the radiation pattern of an antenna.	**4**	**2**	**7**
		OR			
8.	**a).**	Explain one method of measurement of antenna gain.			
	b).	Explain the method of measurement of polarization of an antenna.			
		UNIT-V			
9.	**a).**	Derive an expression for the refractive index of the Ionosphere**.**	**5**	**3**	**7**
	b).	Explain ground wave propagation in detail.	**5**	**2**	**7**
		OR			
10.	**a).**	Derive an expression for the field strength of a Space wave.	**5**	**3**	**7**
	b).	Explain the terms Critical frequency, MUF and Skip distance.	**5**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

			Course Code: B20EC3103		
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R20**
III B.Tech. I Semester MODEL QUESTION PAPER					
DIGITAL COMMUNICATION					
Electronics and Communication Engineering					
Time: 3 Hrs.				**Max. Marks:70**	
Answer **ONE Question** from **EACH UNIT**					
All questions carry equal marks					
Assume suitable data if necessary					
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Explain about delta modulation (DM) systems and design an Adaptive Delta Modulation system to eliminate the drawbacks generated in the DM system.	**1**	**2**	**7**
	b).	Consider that the signal $cos2\pi t$ is quantized into 16 levels. The sampling rate is 4Hz. Assume that the sampling signal consists of pulses each having a unit height and duration dt. & the pulses occur every $t=k/4sec$, $-\infty < k < \infty$. a. Sketch the binary signal representing each sample voltage. b. How many bits are required per sample?	**1**	**3**	**7**
		OR			
2.	**a).**	Explain about the operation of a PCM system. What is Companding?	**1**	**2**	**7**
	b).	With the help of an example explain about the operation of synchronous TDM-PCM system(T1-Digital System)	**1**	**3**	**7**
		UNIT-II			
3.	**a).**	Explain how a binary signal can be transmitted and received by using a BPSK system?	**2**	**2**	**7**
	b).	With the help of an example, explain the method of generating a phase continuous MSK signal.	**2**	**2**	**7**
		OR			
4.	**a).**	Explain the role of a QPSK transmitter and receiver in serial data transmission and reception	**2**	**2**	**7**
	b).	In a DPSK Receiver, the received bit sequence b(t) is 01101100 then i) Find reconstructed bit sequence d(t) ii) Due to presence of noise b(t) is recovered as 01111100 then detect d(t) and identify the bits which are wrongly detected. Use EX-OR logic.	**2**	**3**	**7**
		UNIT-III			

5.	**a).**	Explain about linear filtering and calculate noise power output of RC low pass filter, differentiator and an integrator	**3**	**2**	**7**
	b).	Explain about frequency domain representation of noise. Define noise power spectral density.	**3**	**2**	**7**
		OR			
6.	**a).**	Explain some sources of noise and narrow band representation of noise.	**3**	**2**	**7**
	b).	What is the effect of filtering on power spectral density of noise and obtain the relation between H(f) ,i/p noise psd Gni(f) & o/p noise PSD Gno(f)	**3**	**2**	**7**
		UNIT-IV			
7.	**a).**	What is the function of a baseband signal receiver and derive its probability of error ?	**4**	**3**	**7**
	b).	By deriving expression for Pe for BPSK and BFSK systems, compare the performance of these two data transmission systems.	**4**	**3**	**7**
		OR			
8.	**a).**	Derive the expressions for Probability of error Pe and transfer function H(f) for an optimum filter	**4**	**3**	**7**
	b).	A signal is either $S_1(t) = A \cos 2\pi f_o t$ or $S_2(t) = 0$ for an interval $T=n/f_o$,with n being an integer. Find the error probability Pe of thematched filter.	**4**	**3**	**7**
		UNIT-V			
9.	**a).**	Derive the expressions for output SNR when the binary signal is transmitted using BPSK in a PCM system	**5**	**3**	**7**
	b).	Compare the noise performance of PCM and DM systems	**5**	**2**	**7**
		OR			
10.	**a).**	How a CDMA system uses DS Spread Spectrum to provide multiple access communication.	**5**	**3**	**7**
	b).	Explain the methods of generating PN sequence.	**5**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

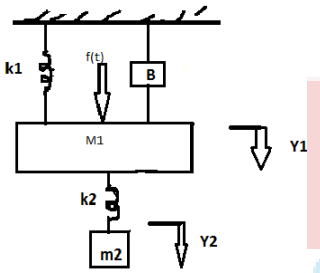
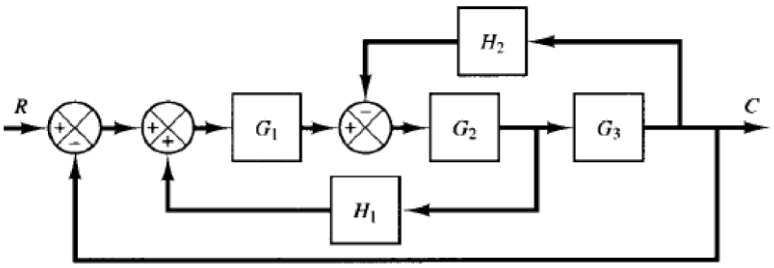
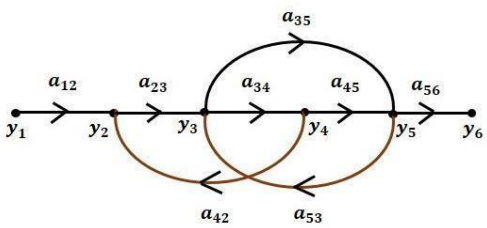
NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

		Course Code: B20EC3104			
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R20**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		DATA COMMUNICATIONS AND COMPUTER NETWORKS			
		Electronics and Communication Engineering			
Time: 3 Hrs.				**Max. Marks:70**	
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Explain various signal encoding methods and write NRZ codes and RZ codes for the following data streams 01011010 and 11001011.	**1**	**2**	**7**
	b).	Discuss various types of MODEM's and explain with block schematic diagram DPSK modulator and demodulator	**1**	**3**	**7**
		OR			
2.	**a).**	Explain various types of data multiplexers and write about Statistical Time Division Multiplexer.	**1**	**2**	**7**
	b).	Differentiate the three categories of Networks LAN, MAN and WAN.	**1**	**3**	**7**
		UNIT-II			
3.	**a).**	Explain the need for layered architecture.	**2**	**3**	**7**
	b).	Determine which of network topologies is the most cost effective for setting up a LAN. Explain the reasons.	**2**	**2**	**7**
		OR			
4.	**a).**	Compare connection oriented and connectionless service.	**2**	**3**	**7**
	b).	Compare the functions of Network layer and Data link layer of OSI model in transferring data between source and destination separated by multiple networks.	**2**	**2**	**7**
		UNIT-III			
5.	**a).**	The frame received by the receiver is 10111101100. Using the generator polynomial G(x) = + 1, verify if the frame is correct or damaged.	**3**	**3**	**7**
	b).	With a neat flow diagram explain the selective repeat ARQ protocol.	**3**	**2**	**7**
		OR			
6.	**a).**	Describe various CSMA protocols. Compare their throughput performance.	**3**	**3**	**7**
	b).	Describe the MAC sub layer frame format of IEEE standard 802.4.	**3**	**2**	**7**

		UNIT-IV			
7.	**a).**	Distinguish the characteristics of virtual circuit and Datagram subnet.	**4**	**2**	**7**
	b).	Differentiate the working of ethernet switch and router.	**4**	**3**	**7**
		OR			
8.	**a).**	Explain the operation of Leaky Bucket Algorithm. Determine its advantages over the Token Bucket Algorithm.	**4**	**3**	**7**
	b).	Explain about IPV4 Addressing Scheme.	**4**	**2**	**7**
		UNIT-V			
9.	**a).**	Explain about elements of Transport protocols.	**5**	**2**	**7**
	b).	Explain the operation of UDP with the help of its header format. List the applications.	**5**	**2**	**7**
		OR			
10.	**a).**	Describe the main function of DNS.	**5**	**2**	**7**
	b).	Explain about the World wide web.	**5**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

					Course Code: B20EC3105
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R20**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		CONTROL SYSTEMS			
		Electronics and Communication Engineering			
Time: 3 Hrs.					**Max. Marks: 70**
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Differentiate open-loop and closed loop control systems with examples.	**1**	**3**	**7**
	b).	For the given mechanical system, obtain the transfer function, $Y_1(s)/F(s)$ and draw its electrical analog based on f-i analogy. 	**1**	**4**	**7**
		OR			
2.	**a).**	Find the transfer function C/R for the following system by using block diagram reduction technique 	**1**	**3**	**7**
	b).	Obtain the transfer function y_6/y_1 for the given SFG using Mason's gain rule. 	**1**	**3**	**7**

		UNIT-II			
3.	**a).**	Distinguish between type and order of a system. What are the various error constants and how they are related to the type of the system?	**2**	**3**	**7**
	b).	Derive the expression for unit-step response of a standard second-order system which is under-damped. Also, describe the transient response specifications	**2**	**4**	**7**
		OR			
4.	**a).**	Discuss the standard input signals used to test control systems. Which one is used mostly and why?	**2**	**3**	**7**
	b).	A unity feedback system is characterized by an open-loop transfer function G(s) = K/S(S+10). Determine the value of gain K such that the system has a damping ratio of 0.5. With this value of K, find the settling time, percent overshoot and steady state error for a unit-ramp input.	**2**	**4**	**7**
		UNIT-III			
5.	**a).**	Explain why all the poles of a closed loop system must lie in the left-half of the s-plane for the system to be stable.	**3**	**3**	**7**
	b).	Using R-H criterion, find the range of K for the closed loop system to be stable. The open loop transfer function of the system is $G(S)H(S) = \frac{K}{S(S+1)(S+2)}$	**3**	**4**	**7**
		OR			
6.	**a).**	Explain how 'Relative stability' of a system can be assessed using RH criterion?	**3**	**3**	**7**
	b).	Obtain the Root-locus for the system with $G(S)H(S) = \frac{K}{S(S+4)(S^2+4S+8)}$ What value of K makes the closed loop system marginally stable?	**3**	**4**	**7**
		UNIT-IV			
7.	**a).**	What are the frequency domain specifications? A second order system step response shows 25% overshoot. What is its resonant peak in frequency response?	**4**	**3**	**7**
	b).	Obtain the Bode plots for the system having OL transfer function $G(S)H(S) = \frac{2500}{S(S+5)(S+50)}$ Determine the Gain Margin and Phase Margin.	**4**	**3**	**7**
		OR			
8.	**a).**	The open loop transfer function of a unity feedback system is given by $G(S) = \frac{1}{S(1+S)(1+2S)}$ .Sketch the polar plot.	**4**	**4**	**7**

	b).	Draw Nyquist diagram and determine the stability of a closed loop control system with open-loop transfer function $G(S)H(S) = \frac{3}{S(S+1)^2}$	**4**	**3**	**7**
		UNIT-V			
9.	**a).**	Construct the SS model for the following transfer function. $G(s) = \frac{2S+1}{S^2+7S+9}$	**5**	**4**	**7**
	b).	Obtain the transfer function model for the following system $\dot{x} = \begin{bmatrix} -4 & -1.5 \\ 4 & 0 \end{bmatrix} x + \begin{bmatrix} 2 \\ 0 \end{bmatrix} u$ $y = [1.5 \quad 0.625] x$	**5**	**3**	**7**
		OR			
10.	**a).**	Find the state transition matrix for the given system. $\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -2 & -3 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 2 \end{bmatrix} u$	**5**	**3**	**7**
	b).	Test the controllability and observability for the following SS model $\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \\ \dot{x}_3(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & -2 & -3 \end{bmatrix} \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} u(t) \qquad y = [3 \quad 4 \quad 1] x$	**5**	**4**	**7**

		Course Code: B20EC3106			
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R20**
		III B.Tech. I Semester MODEL QUESTION PAPER			
		ELECTRONIC MEASUREMENTS AND INSTRUMENTATION			
		Electronics and Communication Engineering			
Time: 3 Hrs.				**Max. Marks:70**	
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Discuss briefly the different types of static errors of a measuring instrument	**1**	**2**	**7**
	b).	List out different AC voltmeters and explain the working of any one voltmeter in detail.	**1**	**2**	**7**
		OR			
2.	**a).**	Explain the following terms in detail (i) Accuracy (ii) Resolution (iii) Precision (iv) Expected value	**1**	**2**	**7**
	b).	Explain the working of a true RMS voltmeter with the help of a suitable block diagram.	**1**	**2**	**7**
		UNIT-II			
3.	**a).**	What is Thermistor and explain it's importance along with advantages of it	**5**	**2**	**7**
	b).	Explain the principle of operation of strain gauges with the help of neat diagrams.	**5**	**3**	**7**
		OR			
4.	**a).**	Draw the LVDT and explain it's operation in detail.	**5**	**2**	**7**
	b).	What are the modes of operation of piezo electric crystals? Explain in detail.	**5**	**2**	**7**
		UNIT-III			
5.	**a).**	Draw the Block diagram of simple CRO and explain it's working.	**3**	**3**	**7**
	b).	Draw the circuit diagram of Dual trace oscilloscope and explain it's operation in detail.	**3**	**3**	**7**
		OR			
6.	**a).**	Explain the measurement procedure of Lissajous patterns with one example.	**3**	**3**	**7**
	b).	Explain the concept of Digital storage oscilloscope along with circuit diagram.	**3**	**3**	**7**

		UNIT-IV			
7.	**a).**	Explain the operation of Maxwell's bridge and derive the condition for balance of a bridge.	**4**	**2**	**7**
	b).	Draw the circuit diagram of Schering's bridge and explain the operation of it.	**4**	**3**	**7**
		OR			
8.	**a).**	Derive the equations of balance for an Anderson bridge? discuss the advantages of the bridge.	**4**	**2**	**7**
	b).	Draw the circuit of Wein bridge and derive the expression for bridge balance	**4**	**3**	**7**
		UNIT-V			
9.	**a).**	Discuss Square wave and Pulse generator with neat block diagrams.	**2**	**2**	**7**
	b).	Explain the working principle of a harmonic distortion analyzer.	**2**	**3**	**7**
		OR			
10.	**a).**	Illustrate the working of a function generator with a neat block diagram.	**2**	**3**	**7**
	b).	Draw the block diagram of random noise generator and explain with neat waveforms.	**2**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

			Course Code: B20EC3107		
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R20**
III B.Tech. I Semester MODEL QUESTION PAPER					
DIGITAL SYSTEM DESIGN USING HDL					
Electronics and Communication Engineering					
Time: 3 Hrs.				**Max. Marks:70**	
Answer **ONE Question** from **EACH UNIT**					
All questions carry equal marks					
Assume suitable data if necessary					
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	What are levels of Abstraction in VHDL?	**1**	**2**	**7**
	b).	Distinguish between signals and variables in VHDL.	**1**	**2**	**7**
		OR			
2.	**a).**	Explain about concurrent and sequential statements with suitable examples.	**1**	**2**	**7**
	b).	With the help of a block diagram, explain the program structure of VHDL.	**1**	**2**	**7**
		UNIT-II			
3.	**a).**	Realize 16:1 multiplexer with 4:1 multiplexer in VHDL programming.	**1**	**3**	**7**
	b).	Define Flip Flop ? Design any sequential circuit using VHDL programming.	**1**	**3**	**7**
		OR			
4.	**a).**	Design sequential 3-bit counter using VHDL programming.	**1**	**4**	**7**
	b).	Develop VHDL Code for Half Adder and Full Adder	**1**	**4**	**7**
		UNIT-III			
5.	**a).**	Explain verilog Data Types and operators.	**2**	**2**	**7**
	b).	Develop the verilog HDL source code and logic diagram for 1-bit full adder using dataflow style.	**2**	**4**	**7**
		OR			
6.	**a).**	Realize 4-bit full adder in Verilog HDL using structural modeling.	**2**	**2**	**7**
	b).	What are the primitive gates supported by Verilog HDL? Develop the Verilog HDL statements to instantiate all the primitive gates.	**2**	**3**	**7**
		UNIT-IV			
7.	**a).**	Design a negative edge-triggered D-flip flop (D_FF) with asynchronous clear, active high. Use behavioral statements only.	**3**	**4**	**7**

		(Hint: Output q of D_FF must be declared as reg). Design a clock with a period of 10 units and test the D_FF.			
	b).	What are rise, fall and turn-off delays in verilog? How are they specified in verilog?	**3**	**2**	**7**
		OR			
8.	**a).**	With syntax explain conditional branching and loop statements available in Verilog HDL behavioural description.	**3**	**2**	**7**
	b).	Design 4-bit Shift Register using HDL Language	**2**	**4**	**7**
		UNIT-V			
9.	**a).**	Explain the state machine coding.	**3**	**3**	**7**
	b).	Describe BIST with the help of LFSR.	**4**	**2**	**7**
		OR			
10.	**a).**	Design a Modulo -8 counter using a sequential circuit approach using D-flipflop.	**3**	**4**	**7**
	b).	Explain scan- path technique in sequential circuit testing.	**4**	**3**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

			Course Code: B20EC3201		
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R20**
		III B. Tech II Semester Regular Examinations			
		MICROPROCESSORS AND MICROCONTROLLERS			
		Electronics and Communication Engineering			
Time: 3 Hrs.					**Max. Marks:70**
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1		Determine the features and architecture of INTEL 8085 Microprocessor	**1**	**2**	**14**
		OR			
2	**a).**	Explain the addressing modes of 8085 with examples	**1**	**2**	**7**
	b).	Indicate flag register of 8085 microprocessor	**1**	**3**	**7**
		UNIT-II			
3		Draw and explain the functional block diagram INTEL 8086 Microprocessor	**2**	**2**	**14**
		OR			
4	**a).**	Illustrate the generation of a 20-bit physical address in 8086 with an example.	**2**	**2**	**7**
	b).	Draw the flag register of 8086 and explain the function of each flag in detail.	**2**	**2**	**7**
		UNIT-III			
5	**a).**	Draw the programmable register array of 8086 and explain the function of each Register	**3**	**2**	**7**
	b).	Write an 8086-assembly language program to find the largest	**3**	**2**	**7**
		OR			
6	**a).**	Explain any five addressing modes of 8086 with suitable example	**3**	**2**	**7**
	b).	Write an assembly language program for 8086 to find if given number is evenor odd	**3**	**2**	**7**
		UNIT-IV			
7		Outline the features and internal block diagram of 8051 microcontroller	**4**	**3**	**14**
		OR			
8	**a).**	Compare Microprocessors & Microcontrollers	**4**	**3**	**7**
	b).	Outline the internal RAM Structure of 8051 Microcontroller	**4**	**3**	**7**
		UNIT-V			
9	**a).**	Explain addressing modes of 8051 microcontroller with examples	**5**	**2**	**7**
	b).	Explain assembler directives of 8051 microcontroller	**5**	**2**	**7**

		OR			
10	**a).**	Explain the stack memory operation using PUSH and POP instructions,	**5**	**2**	**7**
	b).	Explain with examples arithmetic instructions of 8051 microcontroller	**5**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

		Course Code: B20EC3202			
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R 20**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		DIGITAL SIGNAL PROCESSING			
		Electronics and Communication Engineering			
Time: 3 Hrs.			**Max. Marks:70**		
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1	**a).**	Find the Z-transform of the signal xn=2nun-3nu-n-1 and itsregion of convergence	**1**	**3**	**7**
	b).	Realize the series & parallel canonical realizations of the following digital transfer function XZ=z2+2z+4z-8(z2-0.9z+0.14)	**1**	**3**	**7**
		OR			
2	**a).**	Compute the response of the system yn=0.7yn-1-0.12yn-2+xn-1+xn-2 to the input xn=u(n). Discuss the stability of theabove DT system?	**1**	**3**	**7**
	b).	Find the inverse Z transform of Xz= z2z2-2rzcosθ+r2	**1**	**3**	**7**
		UNIT-II			
3	**a).**	Compute the DFT of the following sequence using Radix–2DIT FFT algorithm. Show the all intermediate stage results: xn={0,1,2,0,2,1,0,2}	**2**	**3**	**7**
	b).	Find the DFT of the sequence x(n) = {3, 2, 5, 4}, Using this result, find the DFT of {25, 20, 15, 10}. State the property of DFT used?	**2**	**3**	**7**
		OR			
4	**a).**	Obtain linear convolution of the two sequences given below using circular convolution x1n=1,2, 3,1 ,x2n=2,3, 0,4, 2	**2**	**3**	**7**
	b).	Compute the inverse DFT of the given sequence X(k) ={8, 0, -8+-4j, 0, 0, 0, -8+4j, 0} using DIF-FFT algorithm	**2**	**3**	**7**
		UNIT-III			
5	**a).**	Compare Chebyshev and Butterworth analog filters ?	**3**	**2**	**7**
	b).	Design digital Butterworth lowpass IIR filter using BLT method. The filter specifications are given by i) -3dB cutoff frequency at 0.5π rad, ii) at least 15dB attenuation at 0.75π rad	**3**	**3**	**7**
		OR			

6	**a).**	Compare Impulse invariance and Bilinear transformation methodsof IIR digital filter design	**3**	**2**	**7**
	b).	Convert the following analog filter with transfer function using impulse invariance method HaS=s+0.2s+0.2)2+25	**3**	**3**	**7**
		UNIT-IV			
7	**a).**	Design a linear-phase low pass FIR digital filter to meet the following specifications: (i) Pass band = 0 to 10 kHz (ii) Sampling frequency = 100 kHz(iii) Filter order =10. Compute the impulse response of the desired FIR digital filter using Hamming window	**4**	**3**	**7**
	b).	What is Gibb's phenomenon? Discuss the selection criteria ofwindows with respect to FIR filter design	**4**	**2**	**7**
		OR			
8	**a).**	Show that FIR filters provide constant group delay and phase delay?	**4**	**2**	**7**
	b).	Design a linear-phase band pass FIR digital filter to meet the following specifications: (i) Pass band = 100Hz to 200Hz (ii) Sampling frequency = 1000Hz (iii) No. of samples =11. Compute the impulse response of the desired FIR digital filter using Rectangular and Hamming windows.	**4**	**3**	**7**
		UNIT-V			
9	**a).**	Explain how Sub band coding of speech signals reduces the bit rate .	**5**	**2**	**7**
	b).	Illustrate the operation of up-sampler, down-sampler, Interpolator and Decimator in time and frequency domains with neat sketches	**5**	**2**	**7**
		OR			
10	**a).**	Discuss the effects of finite word length registers.	**5**	**2**	**7**
	b).	Explain about DTMF signal detection	**5**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

		Course Code: B20CE3203			
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R 20**
		III B.Tech. II Semester MODEL QUESTION PAPER			
		VLSI DESIGN			
		Electronics and Communication Engineering			
Time: 3 Hrs.				**Max. Marks:70**	
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Explain the CMOS fabrication steps with neat diagrams.	**1**	**2**	**8**
	b).	Write a Brief note on Various aspects of MOS transistor threshold voltage.	**1**	**2**	**6**
		OR			
2.	**a).**	With neat diagrams explain the process of N-well CMOS Inverter.	**1**	**3**	**8**
	b).	Compare CMOS , BiCMOS and Bipolar technologies.	**1**	**3**	**6**
		UNIT-II			
3.	**a).**	Draw the stick diagrams and layouts for (a)Y=(A+BC) (b)CMOS inverter (c)2 Input NAND and NOR gates	**2**	**2**	**8**
	b).	Define Buried contact, Butting contact and Via contact.	**2**	**2**	**6**
		OR			
4.	**a).**	With a neat sketch, Explain 1.2µm Double Metal, Double Poly CMOS rules	**2**	**3**	**7**
	b).	Draw the layout diagram for OAI logic using CMOS.	**2**	**2**	**7**
		UNIT-III			
5.	**a).**	Write a note on the concept of Sheet Resistance applied to MOS transistors and Inverters with an example.	**3**	**2**	**7**
	b).	Explain various limitations of scaling.	**3**	**3**	**7**
		OR			
6.	**a).**	What are Scaling models and derive all scaling factors for device parameters.	**3**	**2**	**7**
	b).	Calculate total on resistance of CMOS inverter where $Z_{PU}/Z_{PD}=8/1$	**3**	**2**	**7**
		UNIT-IV			
7.	**a).**	Sketch a 3 input NAND and NOR gate using Ratioed and Pass transistor logic	**3**	**4**	**7**

	b).	Write a short note on Bi-stability principle.	**3**	**2**	**7**
		OR			
8.	**a).**	Explain Master-Slave (edge-triggered) S-R flip-flop	**3**	**3**	**7**
	b).	Give a brief explanation about Latches and registers.	**3**	**2**	**7**
		UNIT-V			
9.	**a).**	Explain the basic FPGA Architecture	**4**	**3**	**7**
	b).	Write a short note on Built-in self test (BIST).	**4**	**2**	**7**
		OR			
10.	**a).**	Write various steps to be followed for test mode in Scan Design Techniques?	**4**	**2**	**7**
	b).	Explain the Internal Architecture of Xilinx XC4000.	**4**	**3**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE : Questions can be given as A,B splits or as a single Question for 14 marks

					Course Code: B20HS3202
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R20**
III B.Tech. II Semester MODEL QUESTION PAPER					
UNIVERSAL HUMAN VALUES-2 : UNDERSTANDING HARMONY					
(Common to CIVIL, ECE, EEE)					
Time: 3 Hrs.					**Max. Marks: 70 M**
Answer **ONE Question** from **EACH UNIT**					
All questions carry equal marks					
Assume suitable data if necessary					
			CO	**KL**	**M**
UNIT - I					
1.	**a).**	Discuss natural acceptance	**1**	**2**	**7**
	b).	Differentiate prosperity and deprivation	**1**	**2**	**7**
OR					
2.	**a).**	Write a note on physical facilities.	**1**	**2**	**7**
	b).	Deliberate the right understanding in perspective to self exploration.	**1**	**2**	**7**
UNIT – II					
3.	**a).**	Illustrate coexistence of "I" and "Body ".	**1**	**2**	**7**
	b).	Explain doer, seer and enjoyer.	**1**	**2**	**7**
OR					
4.	**a).**	Discuss Characteristic activities of Harmony with "I".	**1**	**2**	**7**
	b).	Explain Sanyam and Health.	**1**	**2**	**7**
UNIT – III					
5.	**a).**	Write a note on human-human relationship as regarding harmony.	**2**	**2**	**7**
	b).	Differentiate intention and competence.	**2**	**2**	**7**
OR					
6.	**a).**	Discuss salient values in relationship.	**3**	**2**	**7**
	b).	Illustrate universal Harmonious Society - an Undivided society.	**3**	**2**	**7**
UNIT – IV					
7.		Discuss orders of life in nature and its significance self-regulation of individual	**4**	**2**	**14**
OR					
8.		Illustrate existence of human being as coexistence with universe in perspective of space	**4**	**2**	**14**
UNIT – V					
9.		Discuss importance of professional competence for augmenting universal human order.	**5**	**3**	**14**

		OR			
10.	**a).**	Case study of typical holistic technologies.	**5**	**3**	**7**
	b).	Role of engineer in promoting harmony in society	**5**	**3**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

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