Estd:1980

SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE
(AUTONOMOUS)
(Affiliated to JNTUK, Kakinada), (Recognized by AICTE, New Delhi)
UG ProgrammesCE,CSE,ECE,EEE,IT & ME are Accredited by NBA
CHINNA AMIRAM (P.O):: BHIMAVARAM :: W.G.Dt., A.P., INDIA :: PIN: 534 204

Regulation: R20

ELECTRONICS AND COMMUNICATION ENGINEERING (Honors)

SCHEME OF INSTRUCTION & EXAMINATION
(With effect from 2020-21 admitted Batch onwards)

Course Code	Course Name	Year/ Sem	Cr	L	T	P	Int. Marks	Ext. Marks	Total Marks
B20ECH101	CMOS Digital IC Design	II-II	4	3	1	0	30	70	100
B20ECH201	CPLD & FPGA Architectures and Applications	III-I	4	3	1	0	30	70	100
B20ECH301	Algorithms for VLSI Design Automation	III-II	4	3	1	0	30	70	100
B20ECH401	Design for Testability	IV-I	4	3	1	0	30	70	100
B20ECH501	*MOOCS-I	II-II to IV-II	2	--	--	--	--	--	100
B20ECH601	*MOOCS-II	II-II to IV-II	2	--	--	--	--	--	100
		TOTAL	**20**	**12**	**4**	**0**	**120**	**280**	**600**

*Two MOOCS courses of any ELECTRONICS AND COMMUNICATION ENGINEERING related Program Core Courses from NPTEL/SWAYAM with a minimum duration of 8 weeks (2 Credits) courses other than the courses offered need to be takenby prior information to the concern. These courses should be completed between II Year II Semester to IV Year II Semester

Code	Category	L	T	P	C	I.M	E.M	Exam
B20ECH101	Honors	3	1	--	4	30	70	3 Hrs

CMOS DIGITAL IC DESIGN

(Honors Degree Course in ECE)

Course Objectives:

1.	Introduce about Pseudo NMOS Logic characteristics.
2.	Explain combinational and sequential MOS logic circuits.
3.	Elaborate the basic principles of Dynamic logic circuits.
4.	Explain elementary MOS semiconductor memory circuits.

Course Outcomes: After completion of the course, the student will be able to

S.No	Outcome	Knowledge level
1.	Interpret Pseudo NMOS Logic characteristics.	K2
2.	Analyze the operation and construction of combinational and sequential MOS circuits.	K3
3.	Identify the switching action of Dynamic Logic circuits.	K3
4.	Analyze the elementary MOS semiconductor designs.	K3

SYLLABUS

UNIT-I (8Hrs)	**MOS Design:** Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, CMOS Gate design, Power dissipation in CMOS.
UNIT-II (10Hrs)	**Combinational MOS Logic Circuits:** Introduction, MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.
UNIT-III (10Hrs)	**Sequential MOS Logic Circuits:** Introduction, Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits - Clocked SR Latch,Clocked JK Latch, CMOS D latch, and edge triggered flip-flop.
UNIT-IV (10Hrs)	**Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, CMOS transmission gate logic, High performance Dynamic CMOS circuits.
UNIT-V	**Semiconductor Memories:**

(10Hrs)	Introduction, Read-Only Memory (ROM) Circuits, Design of Row and Column Decoder, Static Read-Write Memory (SRAM) Circuits- SRAM Operation Principles, SRAM Write Circuitry, Dynamic Read-Write Memory (DRAM) Circuits.
Text Books:	
1.	Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2011.
2.	Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", TMH, 3rd Edition, 2011.
Reference Books:	
1.	Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011
2.	Jan M. Rabaey, AnanthaChandrakasan, BorivojeNikolic, "Digital Integrated Circuits – A Design Perspective", 2nd Edition, PHI.
e-Resources:	
1.	https://digitalsystemdesign.in/wp-content/uploads/2018/05/C-MOSkang.pdf
2.	https://kgut.ac.ir/useruploads/1508315874150kru.pdf

			Course Code: B20ECH101		
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R 20**
II B. Tech II Semester MODEL QUESTION PAPER					
CMOS DIGITAL IC DESIGN					
(Honors Degree Course in ECE)					
Time: 3 Hrs					**Max. Marks:70**
Answer **ONE Question** from **EACH UNIT**					
All questions carry equal marks					
Assume suitable data if necessary					
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Explain about Pseudo NMOS Logic Inverter.	**1**	**2**	**7**
	b).	Explain **i)** Gain at gate threshold voltage **ii)** Transient response	**1**	**2**	**7**
		OR			
2.	**a).**	Explain about Pseudo NMOS Rise time, Fall time characteristics.	**1**	**2**	**7**
	b).	Explain CMOS Inverter gate design.	**1**	**2**	**7**
		UNIT-II			
3.	**a).**	Briefly discuss about MOS logic circuits with NMOS loads.	**2**	**2**	**7**
	b).	Describe the design of AOI and OIA gates.	**2**	**3**	**7**
		OR			
4.	**a).**	Design a Full Adder circuit with the help of CMOS logic.	**2**	**3**	**7**
	b).	Explain CMOS transmission gate along with characteristics.	**2**	**2**	**7**
		UNIT-III			
5.	**a).**	Explain the Behavior of bistable elements.	**2**	**2**	**7**
	b).	Explain about clocked SR Latch.	**2**	**3**	**7**
		OR			
6.	**a).**	Explain about clocked JK Latch.	**2**	**2**	**7**
	b).	Briefly discuss about behavior of edge triggered flip-flop.	**2**	**3**	**7**
		UNIT-IV			
7.	**a).**	Discuss the basic principles of Pass Transistor Circuits.	**3**	**2**	**7**
	b).	Explain about CMOS transmission gate logic.	**3**	**2**	**7**
		OR			
8.	**a).**	Explain about Voltage Bootstrapping.	**3**	**2**	**7**
	b).	Describe operation of High-performance Dynamic CMOS circuits.	**3**	**3**	**7**
		UNIT-V			
9.	**a).**	Explain in detail about Dynamic Read-Write Memory (DRAM) Circuits	**4**	**2**	**7**
	b).	Briefly describe Read-Only Memory (ROM) Circuits.	**4**	**3**	**7**

		OR			
10.	**a).**	Explain in detail about Static Read-Write Memory (SRAM) Circuits.	**4**	**2**	**7**
	b).	Draw and explain Row and Column Decoder.	**4**	**3**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 14 marks

Code	Category	L	T	P	C	I.M	E.M	Exam
B20ECH201	**Honors**	**3**	**1**	**--**	**4**	**30**	**70**	**3Hrs**

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

(Honors Degree Course in ECE)

Course Objectives:

1.	Familiarization of various complex programmable Logic devices of different families.
2.	To study Field programmable gate arrays and realization techniques.
3.	To study different case studies using one hot design methods.

Course Outcomes: After completion of the course, the student will be able to

S.No	Outcome	Knowledge level
1.	Outline various architectures and device technologies of PLDs, CPLDs and FPGAs.	K2
2.	Illustrate the SRAM Programmable FPGAs	K2
3.	Interpret Anti-Fuse Programmed FPGAs	K2
4.	Build and analyze the digital circuits using various FPGA classes	K4

SYLLABUS

UNIT-I (10Hrs)	**Introduction to Programmable Logic Devices:** Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD.
UNIT-II (10Hrs)	**Field Programmable Gate Arrays:** Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.
UNIT-III (8Hrs)	**SRAM Programmable FPGAs:** Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.
UNIT-IV (8Hrs)	**Anti-Fuse Programmed FPGAs:** Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.
UNIT-V (8Hrs)	**Design Applications:** A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Text Books:

1.	Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition.

2.	Charles H. Roth Jr, Lizy Kurian John, “Digital Systems Design”, Cengage Learning.
Reference Books:	
1.	John V. Oldfield, Richard C. Dorf, “Field Programmable Gate Arrays”, Wiley India.
2.	Pak K. Chan/Samiha Mourad, “Digital Design Using Field Programmable Gate Arrays”, Pearson Low Price Edition

			Course Code: B20ECH201		
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R 20**
III B. Tech I Semester MODEL QUESTION PAPER					
CPLD and FPGA Architectures and Application					
(Honors Degree Course in ECE)					
Time: 3 Hrs					**Max. Marks:70**
Answer **ONE Question** from **EACH UNIT**					
All questions carry equal marks					
Assume suitable data if necessary					
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	What are complex programmable logic devices? Briefly outline salient features of these devices and applications.	**1**	**2**	**7**
	b).	Draw and explain the architecture of CPLD.	**1**	**2**	**7**
		OR			
2.	**a).**	Explain about parallel adder cell.	**1**	**2**	**7**
	b).	Draw and explain architecture of PLD.	**1**	**2**	**7**
		UNIT-II			
3.	**a).**	Draw and explain the General Block diagram of FPGA	**2**	**2**	**7**
	b).	What are the Applications of FPGAs	**2**	**2**	**7**
		OR			
4.	**a).**	Discuss Speed performance of different FPGAs	**2**	**2**	**7**
	b).	With diagram explain I/O block of FPGA.	**2**	**2**	**7**
		UNIT-III			
5.	**a).**	Show how the Xilinx XC3000 CLB can provide a 1-bit adder-subtractor cell for a parallel adder.	**2**	**2**	**7**
	b).	Explain about Parallel Adder Cell	**2**	**2**	**7**
		OR			
6.	**a).**	What programming technologies are used in FPGA devices SRAM	**2**	**2**	**7**
	b).	Briefly explain about Serial Multiplier with Parallel Addition.	**2**	**2**	**7**
		UNIT-IV			
7.	**a).**	Explain the ACT 2 and ACT 3 Logic Modules.	**3**	**2**	**7**
	b).	Explain the functional behavior of the Actel ACT 1 Logic Module.	**3**	**2**	**7**
		OR			
8.	**a).**	Give examples of fuse link in an array logic for a CPLD	**3**	**2**	**7**
	b).	What are the salient features of ACTEL ACT1 and ACT2 FPGAs?	**3**	**2**	**7**
		UNIT-V			
9.	**a).**	Design a 4 bit Ripple counter using one-hot state machine.	**3**	**4**	**7**

	b).	Compare the ACTEL's Act-1,2,3 performance.	**3**	**4**	**7**
		OR			
10.	**a).**	Explain about fast DMA controllers	**3**	**4**	**7**
	b).	Briefly explain about Decade Counter.	**3**	**4**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 14 marks

Code	Category	L	T	P	C	I.M	E.M	Exam
B20ECH301	**Honors**	**3**	**1**	**--**	**4**	**30**	**70**	**3 Hrs**

ALGORITHMS FOR VLSI DESIGN AUTOMATION

(Honors Degree Course in ECE)

Course Objectives:

1.	Understand the concepts of Physical Design Process such as partitioning, Floor planning, Placement and Routing.
2.	Discuss the concepts of design optimization algorithms and their application to physical design automation.
3.	Understand the concepts of simulation and synthesis in VLSI Design Automation ·
4.	Formulate CAD design problems using algorithmic methods

Course Outcomes: After completion of the course, the student will be able to

S.No	Outcome	Knowledge level
1.	Interpret and formulate the flow of VLSI Design for any application. ·	K2
2	Interpret the Methods for Combinational Optimization Techniques	K2
3	Interpret the algorithms for partitioning, floor planning, placement and routing the digital designs at frontend level & at backend VLSI Design level.	K2
4	Compare the various scheduling algorithms , analyzing and solving the issues related to logic synthesis & verification	K4
5	Interpret the algorithms for partitioning, floor planning, placement and routing the FPGA	K2

SYLLABUS

UNIT-I (10Hrs)	**PRELIMINARIES:** Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.
UNIT-II (10Hrs)	**General Purpose Methods for Combinational Optimization:** Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search,
UNIT-III (9Hrs)	**Layout Compaction, Placement, Floor Planning and Routing**:Problems, Concepts and Algorithms. **MODELLING AND SIMULATION:**Gate Level Modelling and Simulation, Switch level Modelling and Simulation.
UNIT-IV (8Hrs)	**LOGIC SYNTHESIS AND VERIFICATION:** Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis. **HIGH-LEVEL SYNTHESIS:**Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations

UNIT-V (8Hrs)	**PHYSICAL DESIGN AUTOMATION OF FPGAs:**FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.
Text Books:	
1.	S.H. Gerez, "Algorithms for VLSI Design Automation", 1999, WILEY Student Edition, John Wiley & Sons (Asia) Pvt. Ltd.
2.	Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, 2005, Springer International Edition.
Reference Books:	
1.	Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", 1993, Wiley.
2.	Wayne Wolf, "Modern VLSI Design: Systems on silicon", 2nd ed., 1998, Pearson Education Asia.

		Course Code: B20ECH301			
SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)					**R 20**
III B. Tech II Semester MODEL QUESTION PAPER					
ALGORITHMS FOR VLSI DESIGN AUTOMATION					
(Honors Degree Course in ECE)					
Time: 3 Hrs					**Max. Marks:70**
Answer **ONE Question** from **EACH UNIT**					
All questions carry equal marks					
Assume suitable data if necessary					
			CO	**KL**	**M**
		UNIT-I			
1.	**a).**	Explain about the most important entities in VLSI Design	**1**	**2**	**7**
	b).	Discuss about Breadth-first search algorithm with examples	**1**	**2**	**7**
		OR			
2.		Explain a design methodology based on top-down structural decomposition and bottom-up layout reconstruction with Y-chart.	**1**	**2**	**14**
		UNIT-II			
3.	**a).**	Explain about Simulated Annealing	**2**	**2**	**7**
	b).	Explain in detail about Genetic Algorithms.	**2**	**2**	**7**
		OR			
4.		Briefly describe the following (i)Local Search and (ii) Tabu search,	**2**	**2**	**14**
		UNIT-III			
5.		With an example explain how high level transformations can be carried out on Data Flow Graphs. What are the advantages and limitations?	**3**	**3**	**14**
		OR			
6.	**a).**	Explain about gate level modelling with examples.	**3**	**2**	**7**
	b).	Explain about switch level modelling with example.	**3**	**3**	**7**
		UNIT-IV			
7.	**a).**	Explain about Allocation, Assignment and Scheduling of Algorithms in high-level synthesis.	**4**	**2**	**7**
	b).	Explain about optimization issues in High-level synthesis.	**4**	**2**	**7**
		OR			
8.		With an example explain how high level transformations can be carried out on Data Flow Graphs. What are the advantages and limitations?	**4**	**2**	**14**
		UNIT-V			
9.	**a).**	Explain about Routing for segmented and staggered Models	**5**	**2**	**7**
	b).	Explain in detail about the design cycle of FPGA's	**5**	**2**	**7**

		OR			
10.	**a).**	Explain about various FPGA Technologies with necessary diagrams.	**5**	**2**	**7**
	b).	What are the various steps in the physical Design cycle of FPGA's? Explain.	**5**	**2**	**7**

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 14 marks

Code	Category	L	T	P	C	I.M	E.M	Exam
B20ECH401	**Honors**	**3**	**1**	**--**	**4**	**30**	**70**	**3 Hrs**

DESIGN FOR TESTABILITY

(Honors Degree Course in ECE)

Course Pre-Requisite(s)

Switching Theory and Logic Design, VLSI Design

Course Objectives:

1.	To give exposure on the Testing, Fault modelling.
2.	To give exposure on Fault simulation and Testability measures.
3.	To give exposure on Built in Self-Test and Boundary Scan Test Instructions

Course Outcomes: After completion of the course, the student will be able to

S.No	Outcome	Knowledge level
1.	Illustrate the fundamentals of Testing	K3
2	Interpret Logic and Fault Simulation	K3
3	Describe the Testability of Combinational Circuits	K3
4	Illustrate the concepts of Built in Self-Test	K3
5	Interpret Boundary Scan Standards in Testing	K3

SYLLABUS

UNIT-I (8 Hrs)	**Introduction to Testing:** Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, Fault Modelling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault - Fault Equivalence, Fault collapsing
UNIT-II (8 Hrs)	**Logic and Fault Simulation:** Simulation for Design Verification and Test Evaluation, Modelling Circuits for Simulation: Modelling levels and types of simulators, Algorithms for True-value Simulation: Compiled code Simulation, Event Driven Simulation.
UNIT-III (10Hrs)	**Testability Measures:** SCOAP Controllability and Observability - Combinational SCOAP measures, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Partial-Scan Design.
UNIT-IV (10 Hrs)	**Built-In Self-Test:** Random Logic BIST: Definitions, BIST Process, Pattern Generation, Built-In Logic Block Observers, Test-Per-Clock, Test-PerScan BIST Systems.
UNIT-V (8 Hrs)	**Boundary Scan Standard:** System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test

	Instructions, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.
Text Books:	
1.	M.L. Bushnell, V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits” Kluwer Academic Publishers.
2.	P.K. Lala, “Digital Circuits Testing and Testability”, Academic Press.
Reference Books:	
1.	M. Abramovici, M. A. Breuer and A.D Friedman, “Digital Systems and Testable Design”, Jaico Publishing House.
e-Resources:	
1.	https://books.google.co.in/books?id=UTrtBwAAQBAJ&pg=PR7&source=gbs_selected_pages&cad=3#v=onepage&q&f=false
2.	https://books.google.co.in/books?id=bw16LHRVH7IC&printsec=copyright&redir_esc=y#v=onepage&q&f=false

				Course Code: B20ECH401	
		SAGI RAMA KRISHNAM RAJU ENGINEERING COLLEGE (A)			**R20**
		IV B. Tech I Semester MODEL QUESTION PAPER			
		DESIGN FOR TESTABILITY			
		(Honors Degree Course in ECE)			
Time: 3 Hrs.					**Max. Marks:70**
		Answer **ONE Question** from **EACH UNIT**			
		All questions carry equal marks			
		Assume suitable data if necessary			
			CO	**KL**	**M**
		UNIT-I			
1	**a).**	Describe Digital and Analog VLSI testing.	**1**	**2**	**7**
	b).	Describe Functional Versus Structural Testing.	**1**	**2**	**7**
		OR			
2		Explain how Stuck-at Fault can be used to cover faults in a system.	**1**	**3**	14
		UNIT-II			
3		Discuss about modelling Circuits for Simulation.	**2**	**2**	14
		OR			
4		Explain the terms a) Compiled code Simulation. b) Event Driven Simulation	**2**	**3**	14
		UNIT-III			
5		With neat diagrams, explain partial-scan design methods.	**3**	**3**	14
		OR			
6		Explain combinational SCOAP measures with a circuit example.	**3**	**3**	14
		UNIT-IV			
7		Explain about BIST process with necessary diagrams.	**4**	**3**	14
		OR			
8		Explain Test-Per Scan BIST System using D flip-flop mode and LFSR mode.	**4**	**3**	14
		UNIT-V			
9		Describe about boundary scan standard instructions.	**5**	**2**	14
		OR			
10		Explain about Boundary Scan Description Language components and pin description.	**5**	**3**	14

CO-COURSE OUTCOME **KL-KNOWLEDGE LEVEL** **M-MARKS**

NOTE: Questions can be given as A, B splits or as a single Question for 14 marks